REMARKS

Claim Rejections

Claims 25-28, 33-34, 36, and 39 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. (U.S. 6,765,152) in view of Jiang et al. (U.S. Pub. 2003/0164556). Claims 29-30 and 35 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. and Jiang et al. in view of Klein et al. (U.S. 2004/0145051). Claim 31 is rejected under 35 U.S.C. §103(a) as being unpatentable over Giri et al. and Jiang et al. in view of Kikuma et al. (U.S. 6,621,169). Claim 32 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. and Jiang et al. in view of Koopmans (U.S. 2004/0035840). Claims 38 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. and Jiang et al. in view of Higgins III (U.S. 5,583,377).

Arguments

As a preliminary matter, Applicant notes that in the outstanding Final Office Action the Examiner has replaced Fjelstad et al. with Jiang et al., but otherwise maintained the prior rejections. As a result, in order to not further burden the record, Applicant chooses to maintain the prior arguments regarding the remaining art and will focus below on the newly cited reference to Jiang et al..

Applicant recites a flip chip package including, *inter alai*, a dummy die having a "metal thermal conducting layer being ***electrically isolated*** from the redistribution layer." Claim 25 (*Emphasis added*). For example, Fig. 4 clearly shows a lack of electrical connections between the metal thermal conducting layer 233 and the redistribution layer 231. In other words, the metal thermal conducting layer 233 is **not** a circuitized layer. *See, also*, p. 6, ll. 9-12. Furthermore, Applicant recites the above flip chip package "wherein the metal thermal-conducting layer is a ***spluttered metal layer***." Claim 39 (*Emphasis added*).

The primary reference to Giri et al. discloses a multi-chip module having chips on two sides including a frame (12), a large semiconductor device (22) located above the thin-film structure, a thin-film structure (18), and a plurality of

semiconductor devices (20) located below the thin-film structure. As admitted on p. 3 of the outstanding Office Action, Giri et al. does not disclose a "dummy die have a metal thermal-conducting layer directly formed thereon."

It follows that Giri et al. do not teach or suggest a flip chip package including a dummy die having an exposed surface located on a bottom thereof, the exposed surface having a metal thermal-conducting layer directly formed thereon to substantially cover the exposed surface located on the bottom of the dummy die, the metal thermal conducting layer being electrically isolated from the redistribution layer. Giri et al. also do not teach or suggest a spluttered metal layer on the bottom surface of a dummy die.

The secondary reference to Jiang et al. is cited as providing this deficiency. In response, Applicant notes that Jiang et al. teaches in [0042], line 1 that the die 10 is electrically connected to the substrate 82 by the conductive trace 104. It clearly follows that the conductive trace 104 is ***electric***. As a result, the reference cannot be said to teach or suggest "the metal thermal conducting layer being electrically isolated from the redistribution layer," as recited in claim 25. Furthermore, with regard to motivation, the skilled artisan would clearly not be motivated to completely defeat the function of the die 10 and conductive trace 104 (i.e., to transmit an electrical signal), and use the die 10 as a non-electrical, thermal conducting layer. Nor does the reference suggest such a modification.

With further reference to Jiang et al. and motivation, Applicant notes that in Figs. 3-4 the die 10 is clearly shown as being connected to the tape or interposer 30 (consisting of core 100 and conductive trace 10) through the die attach layer 80. As a result, the chip 10 is not connected to the tape 30 directly. Accordingly, even if the core 100 is comprised of silicon material, it cannot be said to teach offer Applicant's advantage of the CTE of the dummy die being similar to the CTE of the chip to avoid the warpage of the dummy die connected to the chip 10.

On pp. 4 and 7 of the outstanding Final Office Action, the Examiner has admitted that Giri and Jiang et al. do not disclose "the metal thermal-conducting layer to be a sputtered metal layer...." The Examiner then argues that "sputtered" is a process limitation that Applicant has not shown imparts structural

limitations. In response, as previously noted, Applicant has selected sputtering to form a molecular structure which is particularly suited to heat dissipation (as compared with CVD, ALD, etc). Furthermore, the skilled artisan would clearly understand that a sputtered metal layer yields a certain type of structure having certain depth ranges, formed from certain precursors, and produces a structure having the molecular features of a metal layer which is sputtered (e.g., relatively thick, with high thermal conductivity). Based on the foregoing, Applicant submits that Applicant has met the requisite burden of proof to show that the disclosure of a "metal layer" does not necessarily teach or suggest the structural characteristics of a "sputtered metal layer." Accordingly, Applicant respectfully requests the withdrawal of the rejection of claim 39.

Jiang et al. does not teach or suggest: a flip chip package including a dummy die having an exposed surface located on a bottom thereof, the exposed surface having a metal thermal-conducting layer directly formed thereon to substantially cover the exposed surface located on the bottom of the dummy die, the metal thermal conducting layer being electrically isolated from the redistribution layer. Jiang et al. also do not teach or suggest a spluttered metal layer on the bottom surface of a dummy die.

Neither Klein et al., Kikuma et al., Koopmans, nor Higgins III provide the above-noted deficiencies of Giri et al. or Jiang et al.. Furthermore, Applicant maintains the characterizations and arguments in the Amendment of March 14, 2007 with respect to Klein et al., Kikuma et al., Koopmans, and Higgins III. Applicant further submits that even if the teachings of Giri et al., Jiang et al., Klein et al., Kikuma et al., Koopmans, and Higgins III were combined, as suggested by the Examiner, the resultant combination does not suggest: a flip chip package including a dummy die having an exposed surface located on a bottom thereof, the exposed surface having a metal thermal-conducting layer directly formed thereon to substantially cover the exposed surface located on the bottom of the dummy die, the metal thermal conducting layer being electrically isolated from the redistribution layer; nor does the combination suggest a spluttered metal layer on the bottom surface of a dummy die.

Applicant submits that there is not the slightest suggestion in either Giri et al., Jiang et al., Klein et al., Kikuma et al., Koopmans, or Higgins III that their respective teachings may be combined as suggested by the Examiner. Case law is clear that, absent any such teaching or suggestion in the prior art, such a combination cannot be made under 35 U.S.C. § 103. Applicant further maintains that neither Giri et al., Jiang et al., Klein et al., Koopmans, nor Higgins III disclose, or suggest a modification of their specifically disclosed structures that would lead one having ordinary skill in the art to arrive at Applicant's claimed structure. Applicant hereby respectfully submits that no combination of the cited prior art renders obvious Applicant's pending claims.

Summary

In view of the foregoing remarks, Applicant submits that this application is now in condition for allowance and such action is respectfully requested. Should any points remain in issue, which the Examiner feels could best be resolved by either a personal or a telephone interview, it is urged that Applicant's local attorney be contacted at the exchange listed below.

Respectfully submitted,

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